1 General Information

The DAQ-1101/1102 is a high speed cost-effective data acquisition board that plugs into one of the expansion slots in the IBM™ PC or compatible personal computers. The DAQ-1101/1102 board, shown in Figure 1.1, has capabilities for analog input/output (I/O), digital I/O, and timer/counter functions.

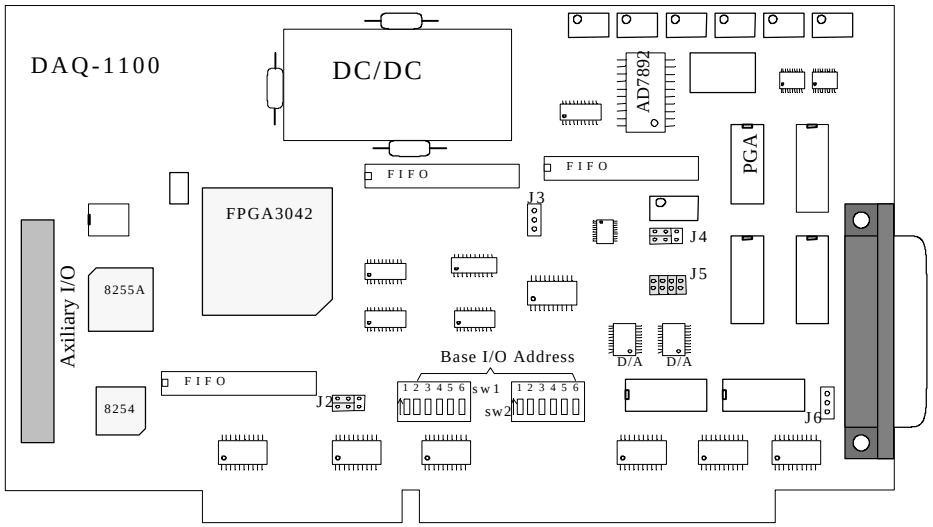

Figure 1.1 DAQ-1101/1102 Board Layout Diagram

The functional block diagram is shown in Figure 1.2.

The analog inputs and outputs, external trigger signal, external reference signal, external clock signal and eight digital inputs and outputs are connected through a 37-pin D-type connector on the board. An auxiliary D-37 connector is employed to support additional 24-bit digital I/O.

The pin diagram of the two D-37 connectors is shown in Figure 1.3.
The difference between DAQ-1101 and DAQ-1102 is that DAQ-1101 is equipped with programmable gain of 1, 10, 100, and 1000, while DAQ-1102 has selectable gain of 1, 2, 4 and 8.

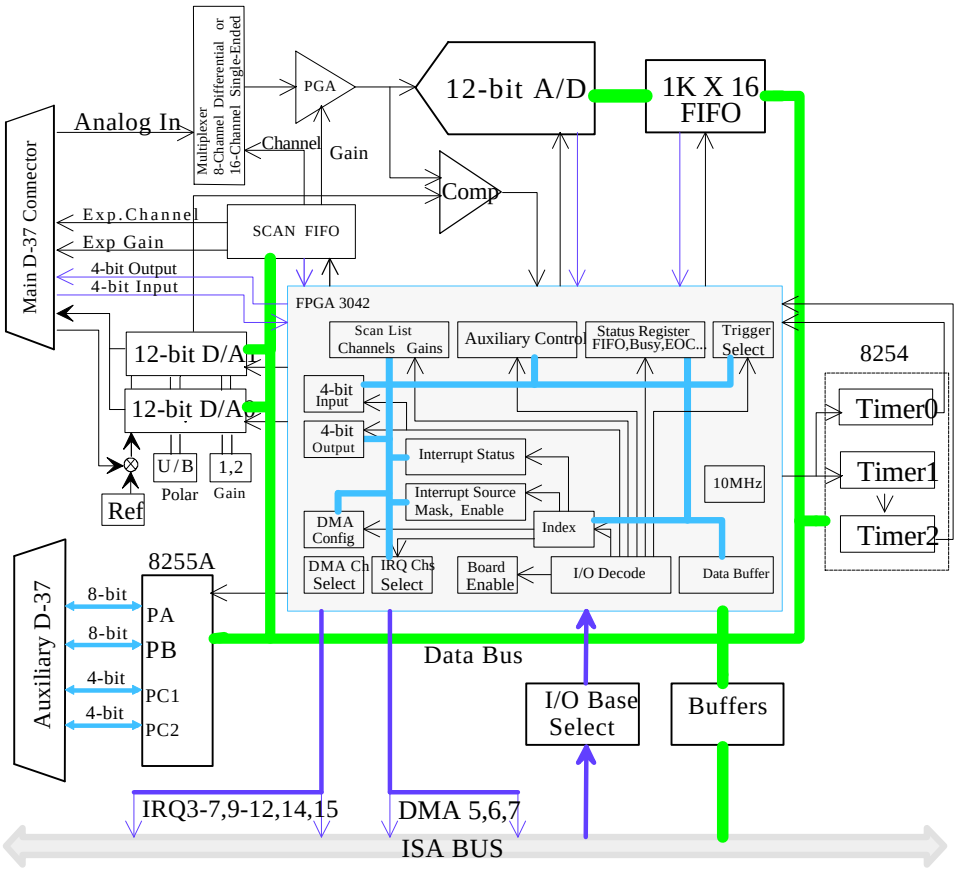

Figure 1.2 DAQ-1101/1102 Block Diagram

1.1 Analog Input Features

The DAQ-1101/1102 contains one high speed 12-bit analog-to-digital converter (ADC), and it supports the measurement of 8 differential input or 16 single ended analog signals. Each differential analog input channel has +/- connections. The single ended analog input channels can be further expanded from 16 to 256 by using four of its digital I/O lines for multiplexing control and the addition of external analog multiplexor card. The selection of the analog inputs from single ended to differential inputs is software programmable. The converter can be configured to receive analog input voltages within the range of 0 to +10V, or ±10V. The analog I/O connections are made via a 37-pin "D" connector on the board. The connector is DAS-1600™ compatible.

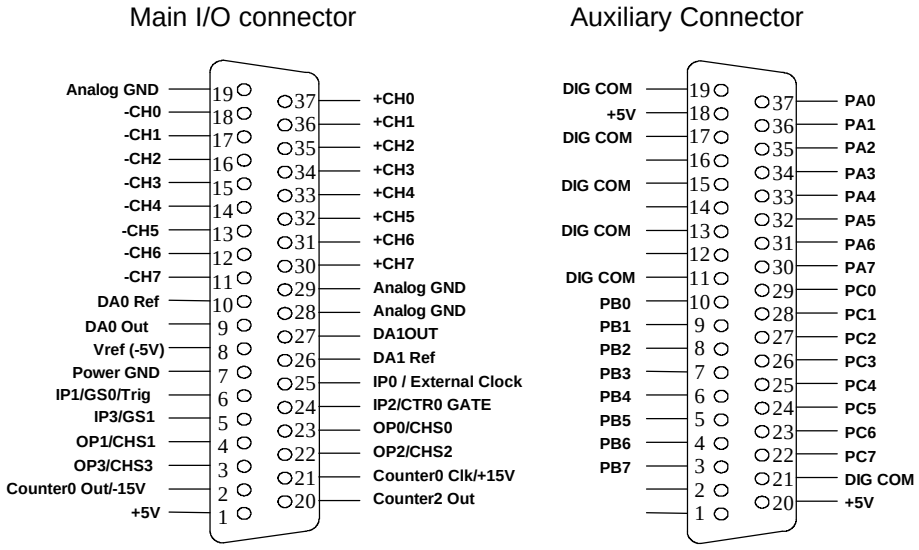

Fig.1.3 D-37 Pin Diagram

The DAQ-1101 provides gains of 1, 10, 100 and 1000, whereas DAQ-1102, gains of 1, 2, 4, 8. Tables below show the voltage's range for a unipolar and bipolar analog input.

DAQ-1101		DAQ-1102	
Input Range	Gain	Input Range	Gain
0 to 10V	1	0 to 10V	1
0 to 1V	10	0 to 5V	2
0 to 100mV	100	0 to 2.5V	4
0 to 10mV	1,000	0 to 1.25V	8

For a gain setting of 1, the 12-bit resolution (4096 counts) provides a least significant bit (LSB) value of 2.44 mV in the 0 to +10V range.

DAQ-1101		DAQ-1102	
Input Range	Gain	Input Range	Gain
-10V to +10V	1	-10V to +10V	1
-1 V to +1V	10	-5 V to +5 V	2
-100mV to +100mV	100	-2.5 V to +2.5V	4
-10mV to +10mV	1,000	-1.25 V to +1.25V	8

For a gain setting of 1, the 12-bit resolution (±2048 counts) provides a least significant bit (LSB) value of ±4.88mV in the ±10V range.

Trigger Source and trigger mode for Analog-to-Digital Conversions

When the DAQ-1101/1102 is powered up, it is in the idle mode and no conversion is performed. The conversion will begin upon receiving a trigger from the user. There are three kind of triggers: the internal trigger, the external trigger, and the analog trigger. The internal trigger is performed by a software program, whereas external trigger is done by hardware. Analog trigger occurs when the input signal exceeds a preset signal set by the user. The preset signal (the threshold voltage) is generated by the output of the second D/A converter. A compare circuit sets off a trigger signal when the input analog signal goes above the threshold voltage. As soon as the board is triggered, A/D will immediately convert the analog signal into a 12-bit digital data, and will be stored into the data FIFO. In addition to internal /external triggering , there is a trigger mode available. The trigger mode is used to decide whether the conversion is done once or multiple times. This also applies to scanning multiple channels whether the scanning is done once or multiple times. The trigger source and the trigger mode are software selectable.

The following summarizes the triggering functions:

(a) Trigger source

- Software trigger
- External TTL trigger with falling or rising edge
- External analog trigger with low to high or high to low transition.

Under the external TTL trigger, the default trigger pin at the main D37 connector is IP0/External Clock (pin 25). However this trigger can originate from the IP1/GS0/Trig (pin 6) if proper selection is made at the index register (see address map in Chapter 5).

(b) Trigger mode .

- Single mode -- one scan for each trigger
- Continuous mode -- Continuous scanning for one trigger

Scan List (Scan FIFO)

One of the functions provided by DAQ-1101/1102 board is the scan list function. The function performs A/D conversion from channel to channel at the highest possible speed. There is a scan FIFO provided on the board

with a depth of 256 points. This scan FIFO is implemented for the scan list function. The scan FIFO contains the channel scan sequence and gains information. At the outset, the scan FIFO must be programmed according to the scan sequence desired. The order of scan sequence must be squential such as 3,4,5,6 .....etc. Gain in conjunction with each channel is also stored into the FIFO. Each FIFO location occupies two bytes. The first byte (low byte) contains the sequence for the extended channels and their gains information (beyond on-board 16 channels), and the second byte (high byte) stores the sequence of on-board channels and their gains. There is a bit in each location in the FIFO (bit 7 of high byte) used to identify the beginning channel. This bit is registered as logic 1 for the beginning sequence and 0 for the others. As the scanning sequence convenes, this bit will tell of the completion of one scan cycle. As soon as the scan list function is asserted, the board will initiate the A/D conversion from the start channel. Right after the conversion is done, the digitized data is entered into the data FIFO and the board selects the next location from the scan FIFO to repeat the same task. This process continues until it reaches the stop channel. For a single trigger mode, it will scan once and stop. For a continuous mode, it will continue scanning at a speed set by the sampling rate, until the desired number of scan times is reached. Up to a 256 channel scan list with individual gain for each channel is programmable in the SCAN FIFO. The scan speed from channel to channel is 2.7 us. This speed is sufficient for the settling time of all the gains except gain of 1000. When you set the gain to 1000 for DAQ-1101, it requires 10 us for the amplifier to settle down. This can be solved by programming the scan FIFO with repeating the same channel-gain four times for each channel. Essentially you slow down the scan speed to 10.8 us for scan list function.

Sampling Rate

When digitizing the analog signal, one of the parameters that must be chosen by the user is the sampling rate. The sampling rate determines how fast the analog signal is digitized. According to sampling theory, the minimum sampling rate must be at least two times the frequency of the input signal. If the sampling rate is two times or higher, the information of the original analog signal can be recovered from the digitized data. The maximum sampling rate of DAQ-1101/1102 is 333KHz. This sampling rate is derived from the 8254 counter/timer chip available on the board. The 8254 has three 16-bit counter/timers. Timer 1 and timer 2 are cascaded to generate the sampling rate pulse. The output of this sampling rate pulse is used for triggering the A/D conversion. The clock input of timer 1 is 10MHz. The counting range of Timer 1 and Timer 2 each is from 2 to 65535, and the sampling period is computed as

Sampling period = Timer 1 data $\times$Timer 2 data $\times$ 100 nanoseconds

The sampling rate in Hz is the inverse of the sampling period. To set the highest sampling rate of 333 KHz, the sampling period must be $\frac{1}{333}$ ms, or 3 us.

Calculation of the values to be filled into the Timer 1 and Timer 2 is as follows:

$$\text{Timer 1 data x Timer 2 data} = \frac{3000}{100} = 30$$

Timer 1 and Timer 2 data should be an integer and their numbers should be ranging from 2 to 65535.

Data FIFO

DAQ-1101/1102 implements a data FIFO (First In First Out) between the output of the A/D converter and ISA bus to buffer the data from the A/D converter output. Unlike the conventional A/D boards where the output digitized data is fetched directly to the PC memory, the output data from the A/D is fed into the FIFO first for temporary storage. The length of the FIFO is 1024 sampling points. The FIFO circuit provides hardware flags for half full, full and empty signals. Utilizing these signals, the board can generate an interrupt to the PC when the FIFO is half full. When the PC is interrupted, the program in the interrupt service routine can use the "STRING" move instruction to move the data in the FIFO directly into the PC memory at a very high speed. In this case, it only interrupt the PC every 512 samples thereby improving the speed of operation. In Windows applications, the latency of the interrupt does not effect the integrity of the digitized data because the data keeps going into the FIFO. Interrupt latency and operation of the data FIFO is mutually exclusive.

The status register (see address map) provides information about FIFO empty, half full and full.

DMA Data Transfer

Another way of transferring the digitized data from the A/D converter to the memory is DMA transfer. The DMA operation is performed by transferring the data at the I/O location directly to the PC memory by-passing the CPU unit. DAQ-1101/1102 implements this DMA transfer. AT style ISA bus has 8-bit DMA transfer channels (1,2,3) and

16-bit transfer channels (5,6,7). DAQ-1101/1102 employs word transfer to improve its speed and efficiency. Selection of DMA channel is software programmable. Proceeding to any DMA transfer, the DMA controller in the PC must be programmed. Information such as the mode of operation, the number of words to be transferred, the memory location etc. must be supplied to DMA controller. After you program the DMA controller, then FPGA will initiate a DMA request to start the operation. When the data transfer is done, a terminal count pulse will be generated by the DMA controller and can be used as a interrupt pulse to inform the PC of the completion of the data transfer. There is a limit of this DMA transfer which the DAQ-1101/1102 can overcome. DMA controller only handles data transfer of 64 K points (one segment). Beyond that, you have to reprogram the DMA controller again. If you are acquiring the data beyond 64K points and sampling at the fast pace, you are bound to miss data points while reprogramming the DMA controller. DAQ-1101/1102 remedies that by utilizing two DMA channels. When one channel is performing DMA operation, the other channel is getting reprogrammed by the user. At the terminal count, the hardware switches the operation to the programmed channel and the completed DMA channel is waiting to be programmed. This Ping-Pong operation guarantees the integrity of the data stream and is only limited by the size of the memory you have in the PC.

1.2 Analog Output Features

In addition to the analog input channels, the DAQ-1101/1102 board contains two analog output channels. Each channel has its own 12-bit digital-to-analog converter (DAC). The analog outputs are buffered and capable of 1 mA current output. The user can select, through jumper setting, the output voltage range for each channel as 0 to +5V, 0 to +10V (Unipolar), or ±5V, ±10V (bipolar). The 12-bit resolution provides LSB value of 4.88mV on the ±10V range and 2.44mV in the 0 to +10V range.

Both channels of digital to analog converters are multiplying DACs. A multiplying DAC requires a reference voltage input in addition to the 12-bit digital values. DAQ1101/1102 provides an internal reference voltage to the multiplying DAC. External reference voltage can also be supplied to the multiplying DAC by jumper configuration.

Analog output has two ways of varying its value: one is I/O write operation and another DMA write operation. DMA for analog output performs faster than I/O operation. Opposite to the DMA analog input function, the DMA for analog output can transfer the data in PC memory to the DAC port at a pace set by the timer. Again Ping-Pong

configuration is made available for DMA output operation which provides the data transfer beyond 64K points. Only one port can be operating at a time.

1.3 Digital I/O

DAQ-1101/1102 has 32 digital I/O lines. Of the 32 lines, 8 of them can be accessed through the main D-37 connector. There are 4 inputs (IP0 - IP3) and 4 outputs (OP0-OP3) as shown in Figure 1.3. The other 24 I/O lines are accessed through a second auxiliary D-37 connector and are generated by a 8255 programmable peripheral interface chip. 8255 has three ports (port A,B,C) and one control register. There are three modes of operations in 8255 determined by the values written into the control register. Mode 0 is for basic input/output configuration where the output port is latched and the input port is not. Any one of the ports can be programmed as input or output. Port C can be further divided into two 4-bit I/O ports . Mode 1 employs Port A or Port B as the data port while using Port C as handshake, interrupt, and digital I/O lines. Mode 2 uses Port A as the bi-directional data port with Port B and C as control and digital I/O applications. For detailed functional description, the reader is referred to the data manual of 8255 by Intel or other manufacturers.

1.4 Counter / Timer

The 8254 counter/timer chip on the DAQ-1101/1102 provides three 16-bit counter/timer channels for time-related applications. Timer 1 and Timer 2 are cascaded together with an input clock of 10 MHz and its output is used for sampling rate application on the board. Timer0/Counter0 is available for the user and connection is provided to the main I/O D-37 connector. Three terminals of counter channel 0 are available through the main I/O D-37 connector.

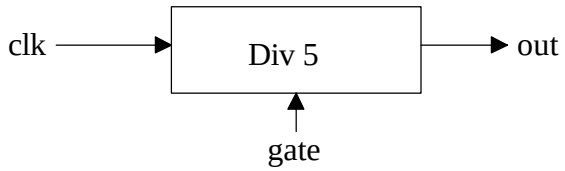

Figure 1.4 Counter Functional Diagram

The three terminals are accessible through Pin 2 (Counter 0 output), Pin 21 (Counter 0 CLK) and Pin 24 (Counter 0 Gate). The functional diagram of the counter is shown in Figure 1.4. The gate terminal should be logic high in order for the counter to function. If gate is held at logic low, the counter is rendered disabled.

1.5 Interrupt

The DAQ-1101/1102 supports AT style ISA bus Interrupts which includes IRQ2-7, 10-12, 14-15. The selection of interrupts is software programmable and is done through the registers setting inside the FPGA. In this particular case, any interrupt conflict can be resolved by moving the selection to another available line without opening the computer case. This facility greatly enhance the convenience for the user if there is a conflict of interrupt selection occurring in the system.

There are five interrupt sources from DAQ-1101/1102 and only one is selected at a time to be connected to the ISA bus interrupt. These interrupt sources are:

- End of scan
- Data FIFO Half Full
- Data FIFO Full
- Timer 0
- Terminal count

The end of scan interrupt is normally used in conjunction with single trigger mode. Right after the scan list is accomplished, the end of scan generates an interrupt to inform the computer to fetch the data. The data FIFO half full interrupt is for continuous trigger mode where the stream of data is getting into the FIFO and whenever the FIFO is half full, it interrupts the PC to fetch at least 512 sample points. This interrupt is very applicable to the Windows environment because of the latency problem inherent in the Windows operating system. The data FIFO full interrupt is not recommended for application unless the interrupt routine is executed promptly before the next data points flow in; Otherwise, an overflow will occur and some data might be lost.

Timer 0 interrupt is used in conjunction with external counter/timer at the main D37 connector. External clock or pulses is connected to clock 0 input and the output of the counter/timer0 can be used for interrupt source. When the user requires to interrupt the PC at a certain time interval, Time 0 can be programmed and meet your requirement.

Terminal count occurs at the end of the DMA transfer of one channel. This interrupt by terminal count will inform the user of the completion of DMA transfer. If the number of the data points is beyond 64K , then the DMA channel must be reprogrammed for Ping-Pong operation.

1.6 Software Supports

The software drivers provide support for various programming languages like Microsoft C/C++, Borland C/C++, QuickBasic, Visual Basic for DOS and Turbo Pascal. A Dynamic Link Library (DLL) is provided for numerous programming languages under Microsoft Windows, as well as the Visual Basic Controls (VBX). Software support can be summarized into four categories:

1) DAQDRIVE Software driver
2) VisualDAQ Visual-Basic Control
3) Labtech Notebook Data acquisition package
4) SnapMaster Data acquisition package

DAQDRIVE is low level driver consisting a set of commands for the user. This generic driver is a library routine for all of Omega's data acquisition board. Programs written for DAQ-1101/1102 can be ported to other boards in the event that the user decides to change the board in the future. DAQDRIVE is available for Window DLL as well as DOS environment. In the case of Visual Basic application, the software provides optional VisualDAQ, which is the visual basic custom control. This software is very useful for graphic presentation and interaction to the hardware data acquisition. Because of the user friendly nature, this software gives a amazing tool to create your own graphic layout.

The last two software packages presented are turn-key system software by Labtech Notebook and Snapmaster. These are menu driven software packages where the user does not need to write their application software. By using the Mouse and key strokes, the data acquisition can be obtained and plotted on the monitor and saved in a file. Post processing of frequency spectrum and other facilities are also available by these two packages. These software packages yield the shortest path to the user to get the system setup and running. No programming is required.

1.7 Power

The DAQ-1101/1102 is powered directly by the ±5V and ±12V power source provided by the computer bus.

1.8 I/O Terminal Strip Connection

The user can connect one or both I/O connectors on the DAQ-1101/1102 board to the external UIO-37 screw terminal panel through a cable assembly as shown in Figure 1.5.

The cable assembly contains a cable for connecting the board to the screw termination panel. The UIO-37 screw termination panel contains two barrier strips, one containing 19 standard slot-head screw terminals, and

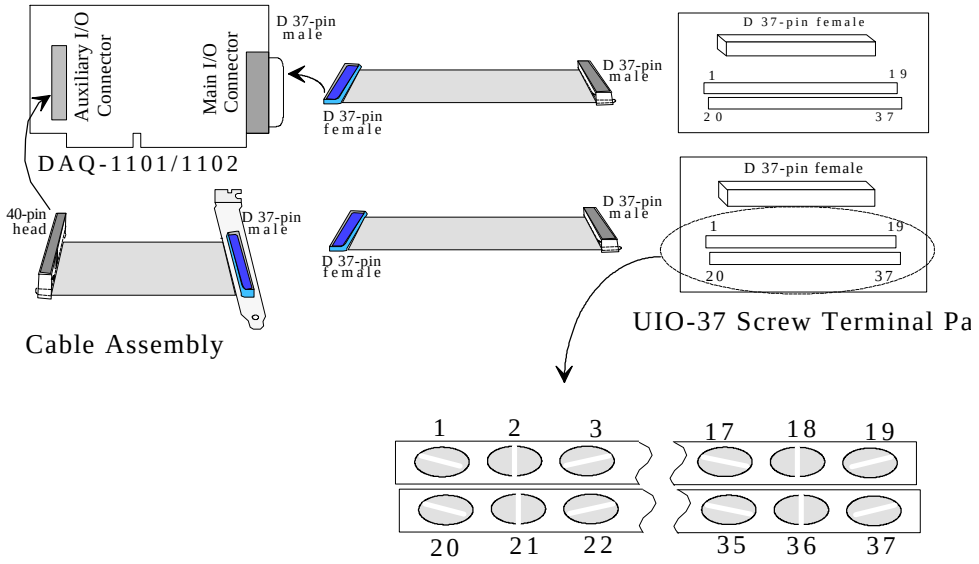

Figure 1.5 I/O Terminal Strip Connector Diagram

another of 18. UIO-37 terminal strip has 37 screw terminal and are labeled from 1 to 37. This number is one to one corresponding to the pin number in D-37 connector at the main and auxiliary connectors. UIO-37 provides easy connection to the external wiring.

1.9 Applications

The DAQ-1101/1102 performs one or several of the following functions: analog input (A/D), analog output (D/A), digital input, digital output and counter/timer. Typical applications of each function are listed in the following:

Analog Input (A/D)
Analog to digital (A/D) conversion converts analog voltage into digital information, which enables the computer to process or to store the signals.

Typical applications are:

- sensor measurement
- waveform acquisition and analysis
- data logging

Analog Output (D/A)

Digital to analog (D/A) conversion is the opposite of A/D conversion. This operation convert the digital information to analog voltage for control of a process, for generating a waveform. Typical applications are:

- process control
- function generation
- pulse train generation

Digital Input/Output

Digital input function is useful in applications such as

- contact closure monitoring
- switch status monitoring

whereas digital output function is useful in

- relay control
- industrial on/off control

Counter/Timer

A Counter/timer is typically used in applications for

- event counting
- pulse generation
- frequency, period and pulse measurement

1.10 Specifications

Analog Input

Maximum Sampling Rate	333KHz
Channels	8 differential, 16 single ended, expandable 256
Input Ranges	-10V to +10V
Output Data Code	Twos complement
Gain Ranges:	
Mode 1101	1, 10, 100, 1000
Mode 1102	1, 2, 4, 8
Input Impedance	1 M ohm
Input Bias Current	50pA
Surge Protection up to	$\pm 20V$
Resolution	12-bit
Conversion Time	1.6us
Conversion type	Successive Approximation
Size of Scan List	256 Samples

Analog Output

Channels	2
Output Ranges	$0-5V, 0-10V, \pm 5V, \pm 10V$
Output Data Coding	Straight Binary
Slew Rate	2.8V/uS
Resolution	12-bit

Digital I/O (8 bits on main D37 Connector)

Output Bits	4
Input Bits	4

Timer/Counter

Number of Counters	3, down
Type	82C54

Digital I/O (24 bits on Auxiliary Connector)	
I/O	24 bits
Type	82C55A
Power Requirements	
+5V DC	800 mA typ, 1,000 mA max
+12V DC	120 mA typ, 160 mA max
Environments	
Operating Temperature	$0 - 70^{o}C$
Interrupt Level	3-7, 9-12, 14, 15
Humidity	0-95%
Dimensions	$8.5in \times 4.8in$

2 Setup

This section describes how to unpack and configure the DAQ-1101/1102 board.

2.1 Unpacking

The DAQ-1101/1102 board is packed in an anti-static bag to avoid possible damage to the ICs on the board. Before removing the product from the bag, touch both the bag and the computer's chassis to establish grounding. After grounding has been established, remove the board and inspect it for signs of damage and loose components. If the board appears damaged, contact Omega Engineering at 1-800-872-9436 immediately.

2.2 Configuring the DAQ-1101/1102

You must decide the appropriate configuration for the DAQ-1101/1102 board depending on your applications. The DIP switch setting SW1, SW2 and Jumper setting J2, J3, J4, J5 and J6 must be selected before installing the board into the computer. While software programmable

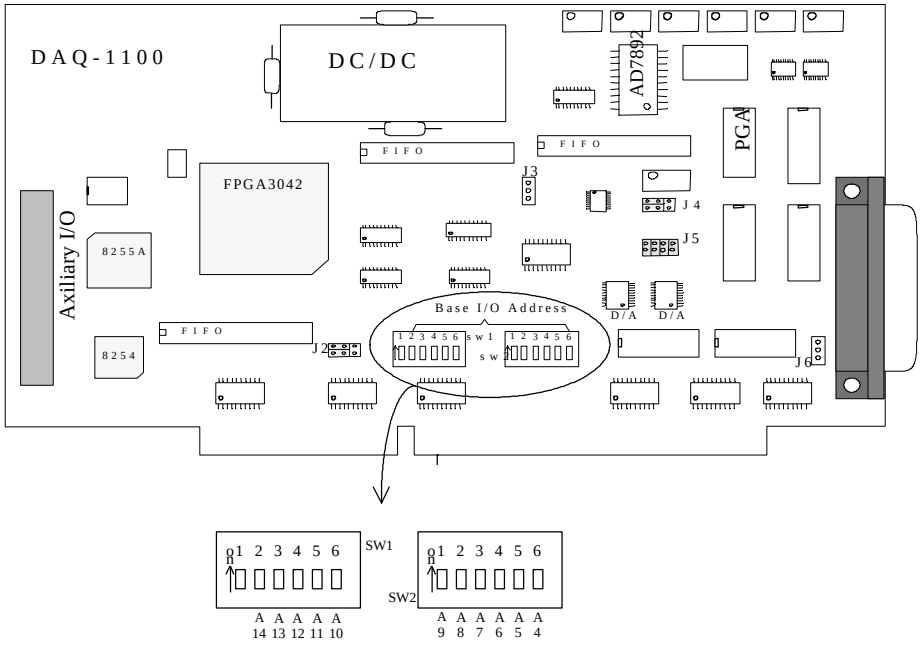

Figure 2.1 Base I/O Address Setting

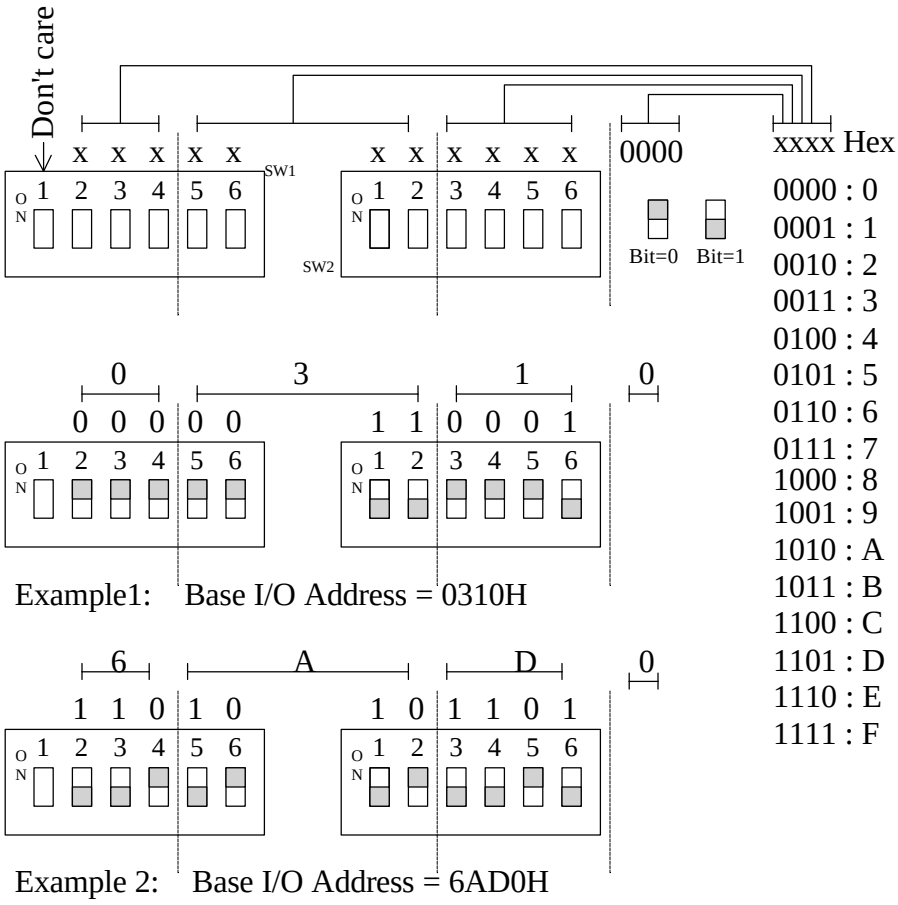

Figure 2.2 Base I/O Address Selection

configurations can be done latter, the following items are jumper or switch configurable and must be decided before installing into the PC:

1. Base I/O address selection
2. D/A voltage reference,bipolar/unipolar output range.
3. internal/external clock source for Timer 0
4. Clock source for A/D converter
5. Counter0 out/ -15 v and Counter 0 Clk/+15v selection

Base I/O Address Selection

Each board inside the PC must have an input/output address. This address is similar to a mail box that the processor of the PC can send the

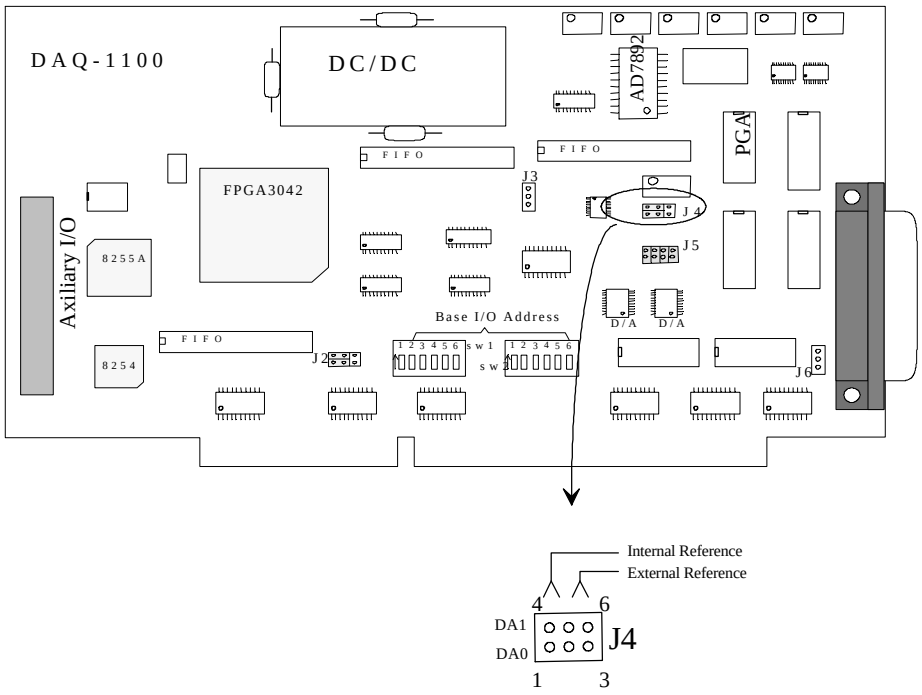

Figure 2.3 D/A Voltage Reference Selection

data to or fetch the data from. Each board has its own unique address that no two or more boards can share the same address. The system uses 16 I/O address lines. The previous IBM machines employed only the first 10 lines for the address selection. Because the 10 lines address locations are limited, the latter machines or add-in boards use more than 10 address lines for address decoding. Some of the I/O locations are pre-assigned and becomes de factor standard locations such as COM1 (3F8H) and COM2 (2F8H). Printer port locations LTP1 and LTP2 are also fixed. I/O address of most other boards are flexible and can be selected anywhere in the I/O space as long as it is not occupied.

The I/O base address of the DAQ-1101/1102 is set using the two DIP switches SW1, and SW2 shown in Figure 2.1. When setting the address selection switches, a switch bit in the "ON" position specifies that the corresponding address line is logic 0. Similarly, a switch in the "OFF" position specifies the corresponding address line to be a logic 1. The I/O base address can be selected from 0000H to 7FF0H with 0010H interval. The upper limit of 7FF0H implies that the address lines involves only 15 lines and the most significant bit A15 is always 0. Switches SW1 and SW2 select address lines A14 through A4. Since the board encompasses 16 register locations requiring 4 address lines A3, A2, A1 A0, only A14

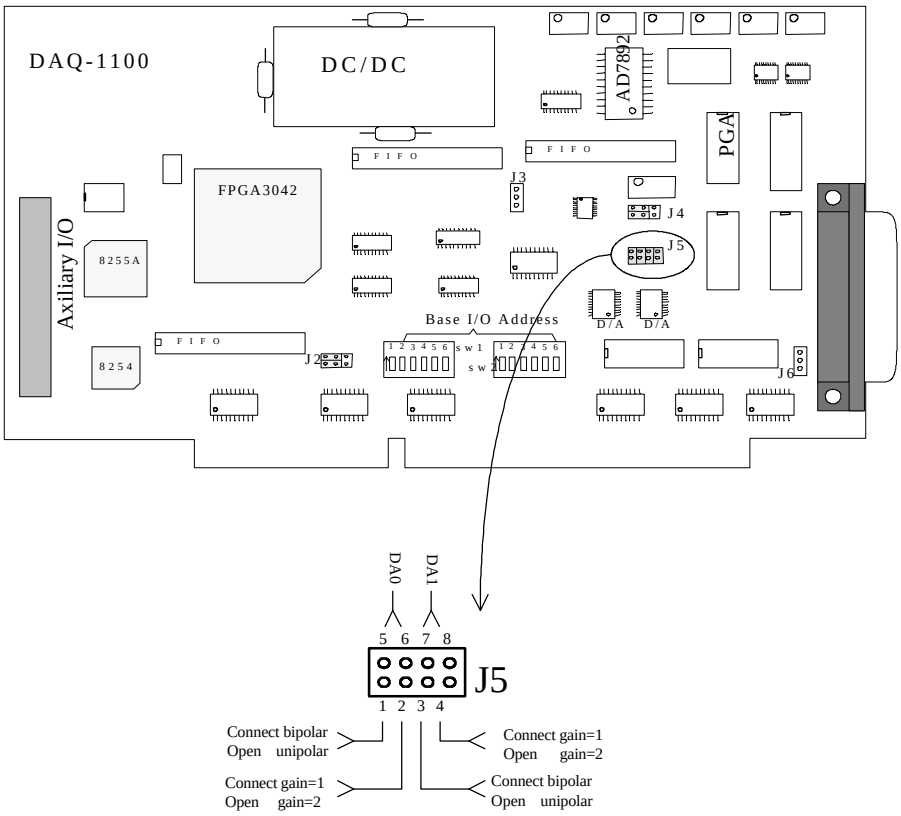

Figure 2.4 D/A Voltage Range and Polar Setting

through A4 address lines are used for base address decoding. Switch SW1 position 2-6 and SW2 position 1-6 are for A14 through A4 address setting. Figure 2.2 shows how the switches on the DAQ-1101/1102 representing different address value.

The default address is set at 300H when shipped from the factory. If you desire to change the factory configuration, use SW1 and SW2 for base I/O address setting. An address of 310H, the SW1 and SW2 setting is shown in Figure 2.2 as Example 1.

D/A Voltage Reference, Bipolar/Unipolar Output Range Selection

The digital to analog converter uses the multiplying DAC AD7945 in the DAQ-1101/1102. The multiplying DAC requires a reference voltage connection to the chip. There are two reference voltage selections

available on the board: one is the internal 5 volt reference voltage and the other from external inputs. Figure 2.3 illustrates internal/external reference voltage selection for DAC channels DAC0 and DAC1. For internal /external reference voltage connection for both DAC0 and DAC1, place jumper at J4:

	DAC0	DAC1
External reference	Pin 2 & 3	Pin 5 & 6
Internal reference	Pin 1 & 2	Pin 4 & 5

Each D/A output offers either Unipolar output or Bipolar output. In addition, the output voltage range also has a choice. The user can choose 5V range output or 10V range output. The 5V range is from the gain selection of 1, whereas the 10V range the gain selection of 2 shown at Jumper 5 header (Figure 2.4). The unipolar or bipolar output selection is made by simply placing the jumper or not placing the jumper at its corresponding location. The tables below demonstrate the combinations of the jumper placement for different requirements.

Pins 1 & 5	Pins 2 & 6	D/A 0 output voltage
Connect	Connect	-5V to +5V, bipolar
Connect	Open	-10V to +10V, bipolar
Open	Connect	0 to +5V, unipolar
Open	Open	0 to +10V, unipolar

Pins 3 & 7	Pins 4 & 8	D/A 1 output voltage
Connect	Connect	-5V to +5V, bipolar
Connect	Open	-10V to +10V, bipolar
Open	Connect	0 to +5V, unipolar
Open	Open	0 to +10V, unipolar

Internal/External Clock Selection For Timer 0

Timer 0 which is made available at the main D37 connector is used for timing application or counting application to the outside circuit. If there is no need to do pulse counting or timing in your application, you can skip this section.

Jumper 2 (Figure 2.5) is used to select internal or external clock. This clock is connected to the clock input of Timer 0. Shorting pins 4 and 5 provides internal 10MHz to counter 0, where pins 5 and 6 can be shorted for external clock provided by the user. When configured as an external input, it can be used for pulse counting for external event.

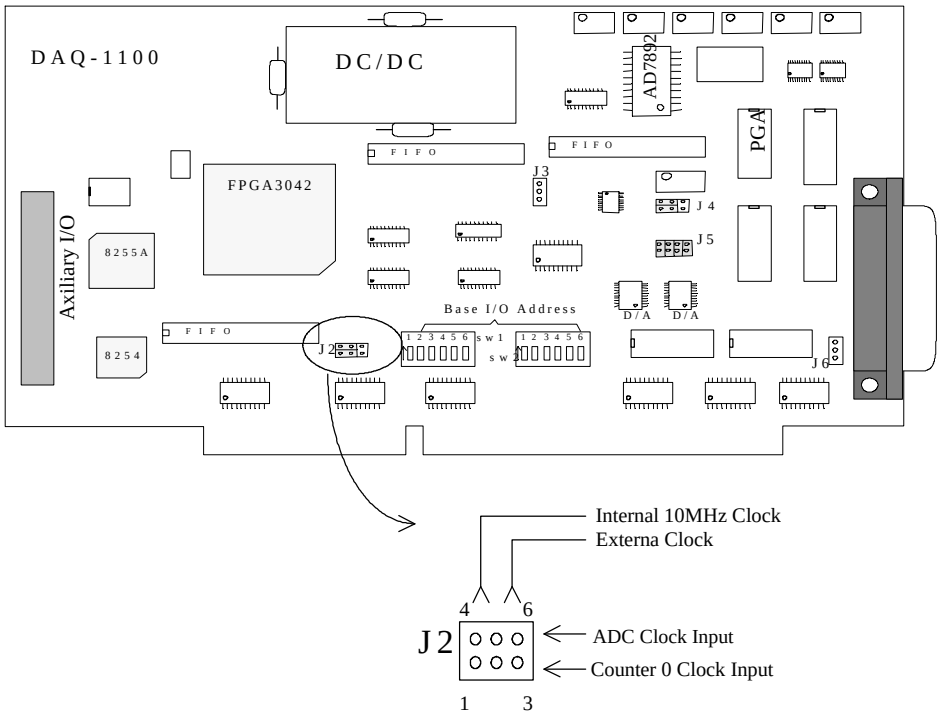

Figure 2.5 Internal/External Clock Selection

Clock source for A/D converter

As mentioned earlier, Timer1 and Timer2 are cascaded together and the output of Timer2 is used for the sampling clock for A/D converter. The sampling rate can be changed by writing different values into the Timer1 and Timer2. The clock input to Timer1 has two different sources: one from the 10 Mhz clock provided on the board and another from the external clock from pin 25 of the main D37 connector. Jumper J2 facilitates this selection.

	Jumper 2
Internal 10Mhz clock	connect pins 1 & 2
External clock	connect pins 2 & 3

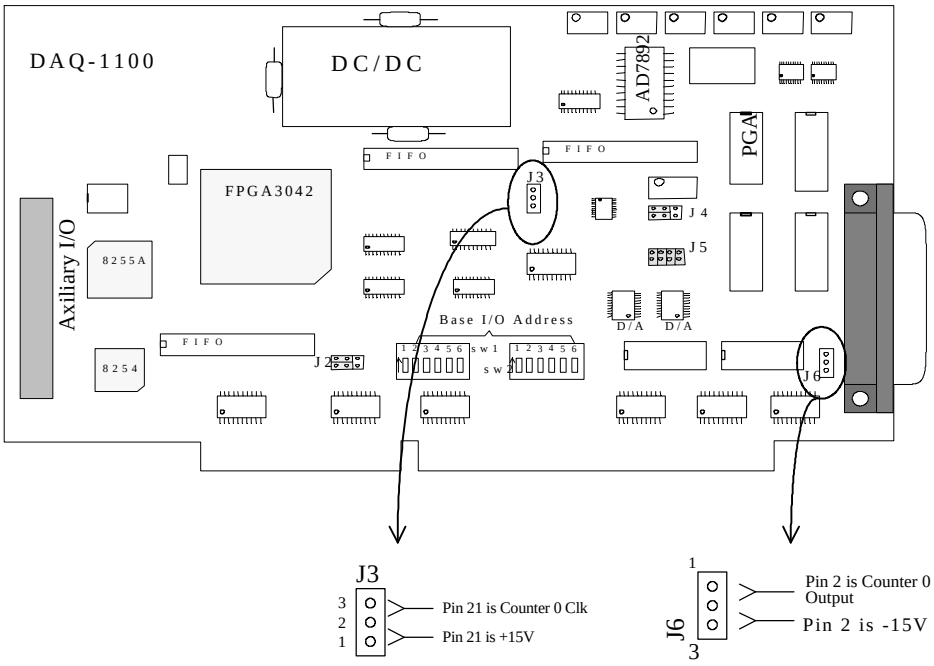

Figure 2.6 Expansion Board Pin Selection

Counter0 Out/-15v and Counter0 Clk/+15v Selection

On the main D37 connector, pin 21 and pin 2 have different functional connections depending on how the jumpers J3 and J6 are configured. If the interest of the user is mainly for counting or timing, then pin 21 and pin 2 at the main D37 connector can be used for Counter 0 output and Counter 0 clock input. On the other hand, the user does not have any application of counting/timing but needs the -15v and +15v output at the D37 connector, DAQ-1101/1102 facilitates this option.

pin 21 & pin 2 at D37 connector	J3	J6
Counter 0 Output Counter 0 Clk	Connect pin 2 & pin 3	Connect pin 1 & pin 2
-15 v and +15 v	Connect pin 1 & pin 2	Connect pin 2 & pin 3

3 Cabling and Field Wiring

Before doing any connection or installation, make sure the computer is off and the power on your external circuit is also off.

Follow the instructions provided by your computer, install the DAQ-1101 or DAQ-1102 board into the computer after finishing the set up in Chapter 2. As shown in Figure 3.1, there are two cables connected from the back of the PC to the UIO-37 terminal strips. As mentioned in Chapter 2, one of the D-37 connector from the back of the PC is main connector on DAQ-1101/1102. The main connector contains all the analog input and output signals. The auxiliary connector which is still D-37 connector in the back of the PC is used for digital I/O connection. Both of the connector and cabling are DAS-1600™ compatible.

UIO-37 is the terminal strip which has number labeled on each position. The numerical number labeled on the terminal strip is corresponding to

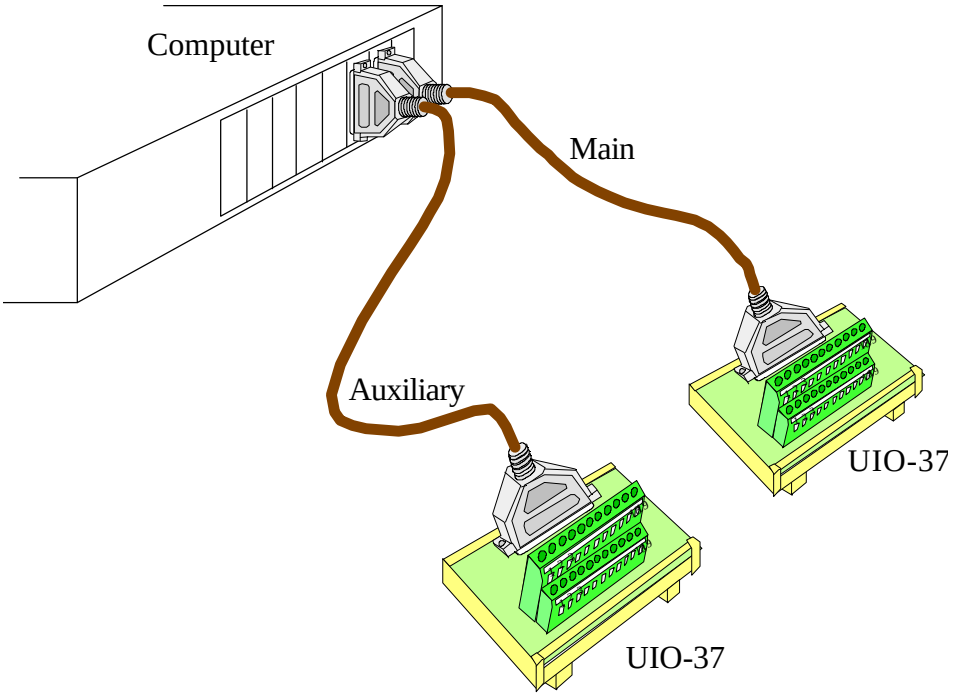

Figure 3.1 Cabling between DAQ-1101/1102 and UIO-37 Terminal Strip

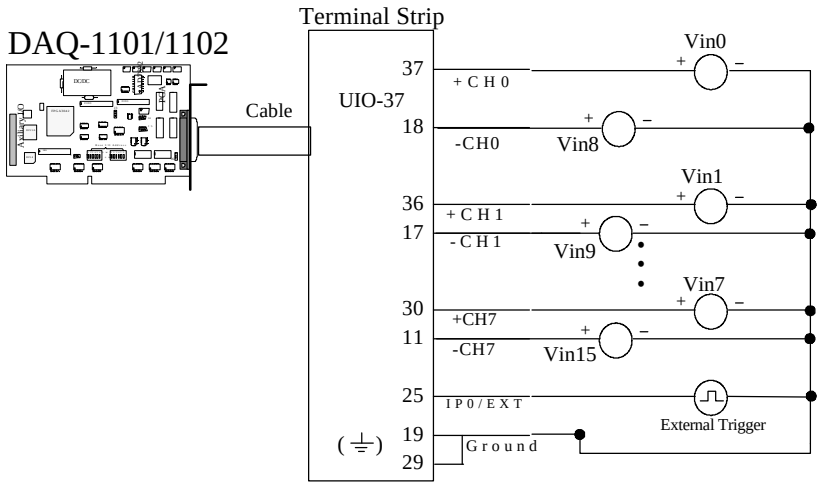

Figure 3.2 Field Wiring for Analog Input with Single ended Configuration

the pin number on D-37 and is one to one correspondence. The wire size recommended for screw terminal connection is gage 16 - 28. After the installation, turn on the computer, then the power on your external circuitry.

3.1 Analog Input Field Wiring

The analog input and output signals reside on the main D-37 connector. The analog signal can have single ended or differential inputs. Figure 3.2 illustrates the field wiring for the single ended inputs. By looking at the main D-37 connector, there are 8 analog input channel with each channel marked with +CHx and -CHx. Single ended signal usually consists of two wires with one input signal wire (+) and another (-) as ground wire. When you do the wiring, connect signal wire with + to the +CHx input, and connect the other wire to ground. Pin 19 and 29 are all analog ground. You can connect all the - wires together and connected to pin 19 and 29 as shown in Fig 3.2.

If a high electrical noise environment exists, individual shielded wiring is recommended. Try to separate the power line and signal lines during installation and never put signal cables and high current or high voltage cable in the same harness. Electromagnetic field or high electric field intensity might deteriorate or interfere with the actual signal that you are measuring.

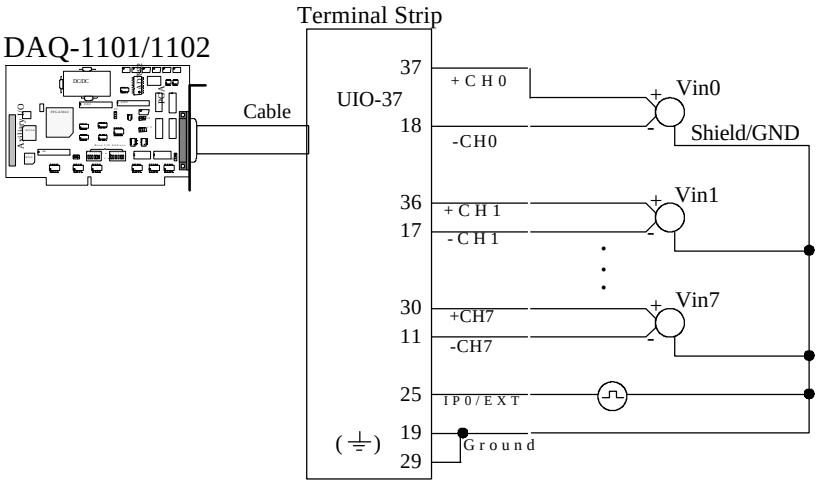

Figure 3.3 Field Wiring for Analog Input with Differential Input Configuratic

For differential input configuration, the input signals normally have three wires: +signal, -signal, and shielded or ground wire. To do differential input field wiring, connect +signal to +CHx and connect -signal to -CHx at the terminal strip (UIO-37). All the shielded or ground wires will be tied together and connected to analog ground of pin 19 and pin 20 at the UIO-37. The advantage of having differential input wiring is that the noise picking up along the +signal and -signal lines will be canceled out at the instrumentation amplifier on the board and leave only the pure signal at the input of the A/D converter. This configuration is assumed to be better than the single ended analog input. As long as the noise level is greater than 1 or 2 LSB, the differential configuration will definitely improve the accuracy of the input signal.

If a sensor output has only two wires with +signal and -signal, no shielded cable is provided, can you connect these two signal wires into differential input field wiring? The answer is yes. You may connect +signal to + CHx and -signal to -CHx. In doing so, the noise induced along the lines will be canceled at the instrumentation amplifier.

Any signal returning wire should not be mixed up with power returning wires, especially for single ended configuration. Signal ground and power ground should not be the same point because the power ground carries current and it might give you noise or offset voltage at the input of the mupltiplexer on the DAQ-1101/1102.

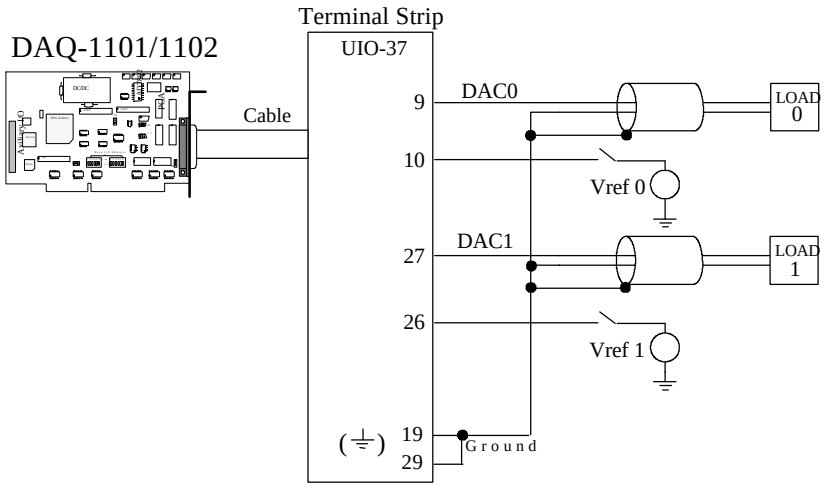

Figure 3.4 Analog Output Field Wiring

3.2 Analog Output Field Wiring

Analog output field wiring is typically shown in Figure 3.4. In this case, two conductor cable with shield is recommended. The positive output is connected to positive terminal which is pin 9 for DAC0 and pin 27 for DAC1. The other terminal and shield are tied together and connected to analog ground of pin 19, pin 29. As mentioned earlier in Chapter 2, the D/A output utilizes internal reference or external reference. If it is an internal reference configuration, no connection is required at pin 10 and pin 26 of their respective reference voltage inputs. However, if the board is configured as an external reference for D/A output, then the external reference voltage must be supplied to it at the terminal strip. The external reference voltage can be a fixed reference voltage or other time varying signal. Since the D/A chip is a multiplying DAC, the output voltage actually is the result of multiplying the D/A output with the reference voltage input. If the reference voltage is fixed, or non time varying, then the reference voltage only affect the magnitude of the output voltage. If the reference signal is time varying signal, then the D/A output signal could become an amplitude modulated signal.

3.3 Counter/Timer Field Wiring

There is a 16-bit counter/timer(Intel 8254 or equivalent) available for the user. The 8254 counter/timer chip has three 16-bit counter/timer. Timer 1 and Timer 2 are cascaded together using 10 Mhz input clock to generate the pacer clock for the A/D function. Only timer 0 is available for the

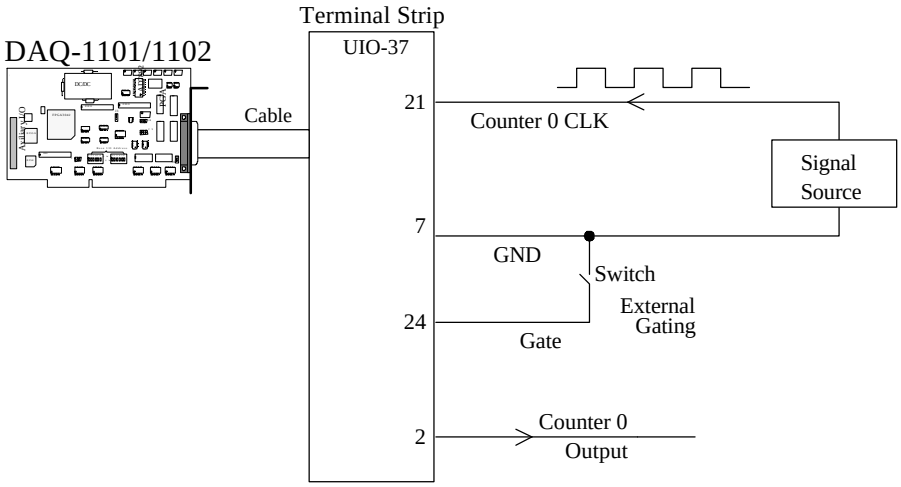

Figure 3.5 Timer/Counter Field Wiring

user. All the control signals, input clock and output clock are made available at the terminal strip or the main D37 connector. This 16-bit counter/timer becomes a timer if input clock is connected to the internal 10 Mhz clock provided on the board (see the jumper configuration on Chapter 2. J4). The output of this timer is taken out at Pin 2. The frequency of this output signal will depend on how the counter is programmed. The gate signal at Pin 24 control the output signal. When the gate is opened, the output at Pin 2 becomes active. When the gate is closed or connected to ground, the output becomes 0. Therefore you can employ this gate signal to control your output clock.

When the jumper configuration at J4 is for external clock, then this 16-bit counter/timer becomes a counter. A counter can be used to count pulses and the result of the counting can be read by the program and into the computer. The signal to be counted is connected to Pin 21. The counting can be enable or disable by controlling the gate signal at Pin 24. If the switch is open, the counter is enable and any pulses coming in at Pin 21 will be counted. The result will be read by the software. If the switch is closed, the counter is disable. No counting occurs even though there are pulses coming in at Pin 21. When the counter overflows, a pulse will be generated at Pin 2 at the output clock.

3.4 Where To Go From Here - Programming

The DAQ-1101/1102 is now configured and ready for use. Depending on the type of application software to be used, the user may wish to review one or more of the following:

1. Chapter 4 of this document provides a basic theory of operation of the adapter for users who wish to learn the technical details about the operation of the DAQ-1101/1102.
2. For users who want to program the adapter with direct I/O transfers to the DAQ-1101/1102 register set, Chapter 5 provides an address map and a detailed description of each I/O register.
3. Users who would like to write custom application software without programming the DAQ-1101/1102 directly should consult the DAQDRIVE software reference manual. DAQDRIVE provides a library of data acquisition subroutines and is included free of charge with the DAQ-1101/1102.
4. For turn-key data acquisition software (i.e. LabTech Notebook or SnapMaster) consult Omega's Data Acquisition catalog for more information.

4 Theory of Operation

4.1 Signal Flow

The block diagram of the signal flow for DAQ-1101/1102 is shown in Figure 4.1. The heart of the architecture of this data acquisition board is contained in Field Programmable Gate Array (FPGA). This FPGA controls all the timing required for A/D conversion, D/A output and

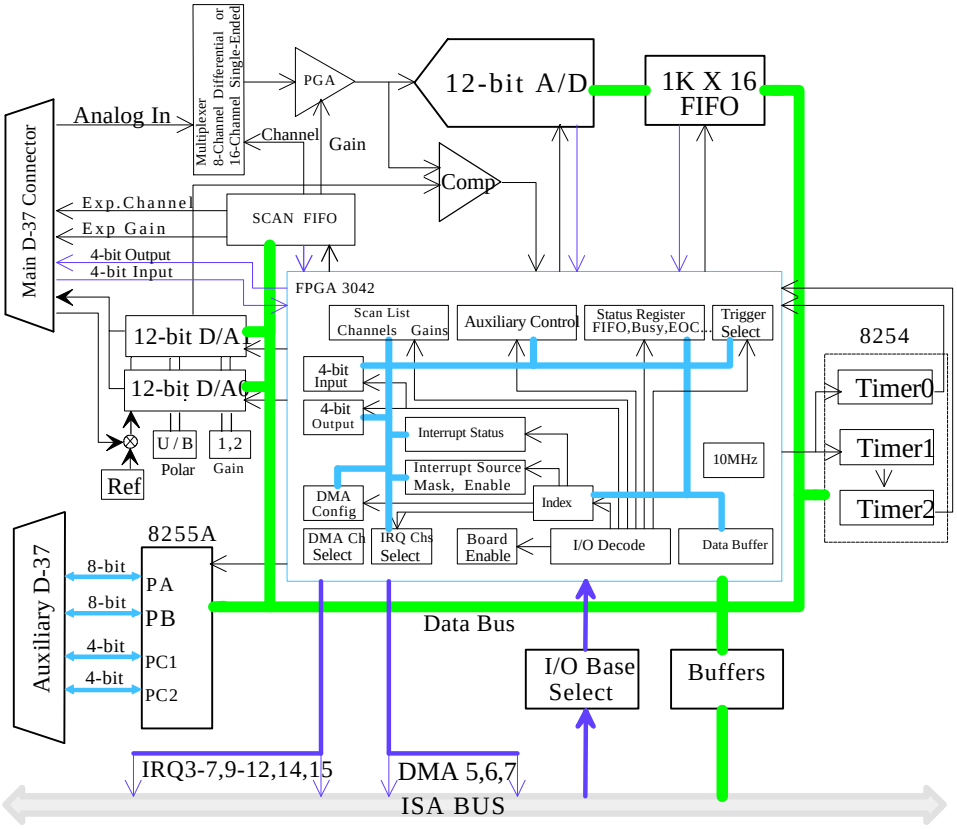

Figure 4.1 DAQ-1101/1102 Block Diagram

digital I/O. There is a common bus on the board which carries the binary data generated by A/D conversion or binary data sent to D/A converter. The data coming in from the digital input port or going out to the digital output port also passes this common bus. The common bus is separated from the ISA bus by a 16-bit data bus buffer.

At the outset, FPGA sends out all the necessary information to select the multiplexer, the gain of each channel, and sampling rate . This is done

by the CPU sending the appropriate data to the registers residing inside FPGA. When these settings are finished, the input signal comes through the analog multiplexer and to the A/D converter via Programmable Gain Amplifier (PGA). The A/D converter initiates the conversion by the command of a signal from FPGA . The output of the A/D converter is a 12-bit binary data and its data format is in 2's complement form. The stream of the A/D output is now fed into a First In First Out 1K X 16 FIFO. The CPU then reads the data from the FIFO. The CPU can read the data after each A/D conversion or CPU can wait until FIFO is half full, then read the data all at once using MOVE STRING operation. Since end of conversion by A/D or FIFO half full , FIFO full and FIFO empty can generate interrupt to the processor, the efficient background data acquisition can be achieved without using polling technique. The FIFO is located at Base +0 address, any read from this location will yield 16-bit data to the CPU. This 16-bit data which is right justified will have upper four bits either 0 or 1 depending on whether it is positive or negative.

The data FIFO should always be flushed prior to the data acquisition. When the FIFO is flushed, or emptied by the host reading all of its content, the empty flag will be set to "1". As long as there is one or more samples left in the data FIFO, the empty flag will be set to "0".

The commencement of A/D conversion is initiated by a trigger from the FPGA. The trigger source can be from the software trigger or external trigger. The software trigger is generated by writing an output command to register Index 2 (see address map in chapter 5). Each time a trigger occurs, a conversion happens and data is generated. One trigger that stimulates one A/D conversion is called single trigger mode. For a continuous mode, the system will be continuously doing A/D conversion at a certain rate after it is triggered. This rate is referred to as sampling rate. The sampling rate is constructed by cascading timer1 and timer2 together with a 10 Mhz clock connected to the clock input of timer1. The rate is determined by how the timer1 and timer2 are programmed. The maximum sampling rate is 333 KHz.

If the analog signal is coming from only one single channel, then the analog multiplexer is fixed. All the converted digitized data will belong to the single analog signal. To observe several channels almost simultaneously, the scan operation must be performed. The scan operation requires specifying the sequences of channel scanning. This is done by writing the words into the scan FIFO. The word consisting of high byte and low byte, contains channel-gain information for the on board 16 channels and expanded channels (external) . Bit 7 of the high

byte is registered as logic one for the beginning channel and will be zero for the remaining channels. The sequence of scanning can be random and up to 256 channels can be programmed. If there is no expanded channels and only 16 channels are used, then all bits of the low byte will be zero. When the scan sequence convenes, the first channel and its gain are read directly from the first location of the scan FIFO with bit 7 of the high byte having logical 1. The trigger signal will start the A/D sampling first and then send a signal to the scan FIFO to switch the multiplexer to the next channel. While waiting for the A/D conversion to finish, the next selected analog signal is settling down at the instrumentation amplifier, therefore, no time is wasted. When the End Of Conversion pulse EOC appears indicating A/D conversion is done, the converted data is written into the data FIFO. The A/D will be start again in ever 2.7us time period. The same process repeats until the end of the channel is reached. The end of the channel is detected by bit 7 of the high byte in the scan FIFO since the beginning channel has a logical 1. For a single trigger mode, the controlled logic in the FPGA will scan once and stop. For a continuous mode, the controlled logic will scan from the start channel to the end channel, and then wait for the next sampling clock. The sampled data is sequentially stored in the data FIFO and read by the processor. You must sort out the data for each channel for the scan mode operation.

D/A operation is simply performed by sending 12-bit data through the data buffer to the selected D/A channel. The strobe signal necessary for latching the 12-bit data to the register inside D/A converter is generated by FPGA. The data sent to Base+8 will go to channel 0 and the data sent to Base+A will go to channel 1.

4.2 Analog Input

DAQ-1101/1102 provides 16 channels single ended or 8 differential analog input channels. The choice of single ended or differential input is done by the software. Selecting one of the 16 channel for A/D conversion utilizes HI-507A as its input multiplexer. The HI-507A multiplexer has input over-voltage protection which protect the analog circuit when transient voltage occurs. The output of the multiplexer is connected to the programmable gain amplifier (PGA) which has a gain of 1,10,100,1000 for DAQ-1101 and a gain of 1,2,4,8 for DAQ-1102. The maximum voltage output of the PGA is limited to +/- 10V. The maximum analog input range at the multiplexer is also +/- 10V, therefore various gains can be selected to optimize the accuracy of the input signal for data conversion. For instance, if you know your input signal falls within +/- 40 mV, you can use DAQ-1101 and set the gain at 100 which will yield the maximum

voltage of +/- 4V at the output of PGA. However, if the signal is only +/- 0.625V at the input, then a gain of 10 can be chosen to give the maximum accuracy. The output of the PGA is then connected to the sampling A/D converter (AD7892).

The A/D converter has a 12-bit 2's complement binary output. The converter type is successive approximation and its conversion time is 2us.

It is strongly recommended that the single-ended/differential selection be the same for all the internal channels (e.g. all 8 channels as differential, or all 16 channels as single ended). A mixed channel configuration, possible as it seems to be, will cause confusion and unexpected signal errors. For expanded channels (beyond 16), all the configuration has to be single ended since the expansion cards can only be used on single ended channels.

4.3 Analog Output

The 12-bit data sent to Base + 8 location by the processor using word transfer will travel from the ISA bus to the internal bus and get to the latch at the D/A converter of channel 0. When the latch receives the new data, it will go through digital to analog conversion and the analog voltage corresponding to the binary value appears. For each binary value, it will get its corresponding analog voltage. The analog output voltage is then buffered through operation amplifier to pin 9 of the main connector. The buffered amplifier is used to increase its output driving capability. Any 12-bit data sent by processor to address Base + A will terminate at the latch of D/A channel 1. The same type of buffered circuit is attached to the output of channel 1 D/A converter.

The AD7945 D/A converter is a multiplying DAC. A reference voltage must be provided to the chip. LM336-5.0 supports this reference voltage and yields a +/- 5V analog output with the buffer stage configured at a gain of 1. When the buffer stage sets the gain to 2, the output will have a maximum of +/- 10V. Jumper configuration can enable the user to select a unipolar output with 0 to 5V or 0 to 10V.

The reference voltage can come from an external circuit by jumper selection. The reference voltage does not have to be a constant voltage. If the reference voltage is a time varying signal, the multiplying this voltage with the D/A output will result with a complex signal. Not only the analog value sent by processor changes, the maximum magnitude also changes. If the reference voltage is not a time varying signal , adjusting

the reference voltage will change the D/A output range. You can customize the D/A output voltage by feeding the appropriate reference voltage.

4.4 Digital I/O

The digital I/O function of DAQ-1101/1102 provides a 4-bit TTL compatible input and a 4-bit TTL compatible output. Both are accessed through the main connector on the board. The digital data flow is controlled by the FPGA. In addition to this 4 bit digital I/O, there is a 82C55 programmable peripheral interface chip on the board which supplements an additional 24 digital I/O lines. The 82C55 is located at Base + C and occupies consecutive four I/O addresses. The 24 bit digital I/O is divided into three 8-bit ports and each port can be configured to be either input or output. There are three modes of operation for 82C55: mode 0 for basic input output, mode 1 for digital I/O with handshake lines and mode 2 for bi-directional data transfer. The mode is determined by the control word of the 82C55 located at Base+F. All three ports are accessed through the second auxiliary connector of D37.

At power up all three ports are configured to be input ports. However, the configuration can be altered by writing a value to the control word register. For detailed discussion of 82C55, refer to data sheet by its manufacturers.

4.5 Counter / Timer

The 82C54 has three counter/timers. Timer1 and Timer2 are cascaded to generate pacer clock or sampling clock. Only counter 0/timer 0 is available for the user. The counter/timer has clock input, gate control input and pulse output. When the gate control signal is low, no counting/timing occurs. DAQ-1101/1102 has a internal pull up at the gate control input. No connection at this gate will equivalently enable the counter. When used as a counter, the content of the counts can be read by the processor. The application includes frequency measurement, event counting etc. When used as a timer, the output pulse rate can be programmed by the processor and its application such as time proportional output, pulse outputs etc. can be realized.

5 Address Map for DAQ-1101/1102

The address map of DAQ-1101/1102 occupies 16 I/O locations. It starts from Base+0 and ends with Base + F. The actual addressable registers in DAQ-1101/1102 are more than 16 locations. This is done by utilizing the index register at Base +2. The contents of the index in the index register will address to different sets of locations when you write or read to Base + 3. The following table illustrates the address map of DAQ-1101/1102.

Base + 0,1	Read 16-bit DATA FIFO Write 8-bit Scan FIFO 1st byte: Gain and Channel setting for Expansion board 2nd byte: Gain and Channel setting
Base + 2	Read 8-bit Index Register Write 8-bit Index Register
Base + 3	8-bit Read/Write Index 0 Configuration register 1 Interrupt level /DMAselection register 2 Auxiliary control register 3 Interrupt enable register 4-7 82C54 counter/timer
Base + 4	8-bit Read/Write Status register
Base + 5	8-bit Read only Interrupt status register
Base + 6	4-bit Read/Write 4-bit digital I/O and expansion control
Base + 7	Reserved
Base + 8..9	16-bit Write only D/A channel 0
Base + A..B	16-bit Write only D/A channel 1
Base + C..F	82C55 8-bit Read/Write
Base + 8000	Read/Write Disable/Enable DAQ-1101/1102

Base + 0,1: Read -- 16-bit data will be read from DATA FIFO into the PC.

This is a 16-bit data transfer. The data format is a 2's complement number. For positive numbers, the 16-bit data format is: 00000XXX XXXXXXXX. For negative numbers, the data format is: 11111XXX XXXXXXXX.

Write to Base+0 is a byte operation.

Sequentially writing 8-bit data to Base+0 will store the data in the scan FIFO. Each scan in the scan list needs two continuous bytes to specify the gains and channels for both main connector and expansion board. The odd byte writing to the scan FIFO specifies the gain and channel for the expansion board, and the even byte writing to the scan FIFO specifies the first scan bit, gain and channel for the main connector.

Each channel has 4 different gain selections (1.2.4.8 or 1.10.100. 1000) and therefore two bits are required for each channel.

EG_{1_0}/GN_{1_0}	DAQ-1101	DAQ-1102
00	1	1
01	10	2
10	100	4
11	1000	8

Even byte D7 D6 D5 D4 D3 D2 D1 D0
(low byte) X X EG_0 EG_1 EC_3 EC_2 EC_1 EC_0
(please note the sequence of EG_0 and EG_1)
EG_{1_0}: Gain selection for expansion board
EC_{3_0}: Channel selection for expansion board

Odd byte D7 D6 D5 D4 D3 D2 D1 D0
(high byte) SOS X GN_1 GN_0 CH_3 CH_2 CH_1 CH_0
GN_{1_0}: Gain selection for main connector
CH_{3_0}: Channel selection for main connector
SOS: flag of Start of the Scan list

Befor programming the scan FIFO, you must flush the FIFO using Index register 2.

Programming for a single channel: write two bytes into the scan FIFO with SOS setting to logic one. The gain for both low byte and high byte prefers to be the same to eliminate the noise.

Example: select the analog input channel 3 with a gain of 10 (EG1 EG_0)

Low byte ------0001 0000

High byte----- 1010 0011

Write 10, A3 into the scan FIFO that will select channel 3 with a gain of 10.

The fastest settling time for a single channel is 3 us or 333Khz sampling rate.

Programming for the multiple channels: write multiple bytes into the scan FIFO with SOS setting to "1" for the start channel and others to be "0". The gain for both low byte and high byte prefers to be the same to eliminate the noise.

Example: scan channel 0 to 3 with the following gains--

Channel	Gain
0	11
1	10
2	01
3	00

The byte sequence written into the scan FIFO are:

X X EG_0 EG_1 EC_3 EC_2 EC_1 EC_0
SOS X $GN_1GN_0CH_3CH_2CH_1CH_0$
0011 0000 1011 0000
0001 0001 0010 0001
0010 0010 0001 0010
0000 0011 0000 0011
or
30 B0 11 21 22 12 03 03

The time it takes to scan from one channel to the next is 2.7 us. This applies to the DAQ1101/1102 with a gain of less than 1000. Choosing a gain of 1000 requires a settling time of 10 us for the amplifier. Therefore the speed of scanning must be slow down. This can be done by repeating the same channel 4 times in the scan FIFO to yield a speed of 10.8 us. Using the above example for instance (i.e. the board is DAQ1101 with gain of 1000), the data written into the scan FIFO is:
30 B0 30 30 30 30 30 30 11 21 11 21 11 21 11 21 22 12 22 12 22 12 22 12 03 03 03 03 03 03 03 03.

Base + 2: Index register

Write: 00000XXX. Write a byte to this location will set an index in the index register. The last 3-bit represents the number of index ranging from 0 through 7.
Read: 11111XXX. The last 3-bit is the index number written.
Indexing operation occupies two I/O location. First writing an index to the index register at address Base+2. If the index is 0, the next byte written to Base +3 will be going to index 0 register.

Base + 3: After writing to index register at Base + 2, the next write to Base + 3 will direct you to different index registers.

Index 0 : Configuration register D7D6D5D4D3D2D1D0
WRITE/READ
D7: 1 -- DMA enable
0 -- DMA disable
D6: Read: Current DMA channel
Write: Multi DMA selection
1 -- multi-channel DMA
0 -- single-channel DMA
D5: Source of DMA request

1 -- DMA source is D/A
0 -- DMA source is A/D

D4: D/A channel selection for DMA
1 -- DMA source is for D/A channel 1
0 -- DMA source is for D/A channel 0

D3: 1 -- digital trigger
digital signal can come from IP0/external clock or from IP1/GS0/Trig (see Base+6,bit D5).
0 -- analog trigger *see example at the end of this chapter.

D2: 1 -- single trigger mode
0 -- continuous mode

D1: 1 -- internal trigger
0 -- external trigger

D0: 1 -- rising edge trigger
0 -- trailing edge trigger

Index 1: Interrupt level/DMA selection register

D7D6D5D4D3D2D1D0 WRITE/READ

D7D6D5D4	IRQ Level
0000	disabled
0001	disabled
0010	disabled
0011	IRQ3
0100	IRQ4
0101	IRQ5
0110	IRQ6
0111	IRQ7
1000	disabled
1001	IRQ9
1010	IRQ10
1011	IRQ11
1100	IRQ12
1101	disabled
1110	IRQ14
1111	IRQ15

D3D2	DMA channel A
00	DMA 5
01	DMA 6
10	DMA 7
11	No DMA

D1D0	DMA channel B
00	DMA 5
01	DMA 6
10	DMA 7
11	No DMA

Index 2: Auxiliary control register , Write only

D7D6D5D4D3D2D1D0

D7: 1 -- software trigger
0 -- no software trigger

D6: 1 -- flushing scan FIFO
0 -- no action

D5: 1-- flushing data FIFO-reset the FIFO pointer
0 -- no action

Note: both data FIFO and scan FIFO must be flushed before application.

D4: not used

D3: setting this bit to "1" will stop the scanning operation in continuous mode (trigger mode: continuous). During the middle of scanning operation, the scanning function will not stop immediately when the bit is set to 1. It will continue A/D conversion until the scanning sequence is done and then it will be stopped. After ceasing operation, the state is still in continuous mode waiting for trigger to occur.

D2: setting this bit to "1" will synchronously disable DMA with next Terminal Count signal TC

D1: not used

D0: not used

Index 3: Interrupt enable register. Write/Read

D7D6D5D4D3D2D1D0

D7: 1 -- global enable (must be 1 for any interrupt)
0 -- disable

D6: not used

D5: 1 -- Terminal Count (TC) enable
0 -- disable

D4: 1 -- Timer0/Counter0 interrupt enable
0 -- disable

D3: 1 -- external trigger interrupt enable
0 -- disable
D2: 1-- FIFO full interrupt enable
0 -- disable
D1: 1 -- FIFO half full interrupt enable
0 -- Disable
D0: 1 -- End of scan interrupt enable
0 -- Disable

Index 4..7: Write/Read 8254 counter/timer
Index 4: Write/Read Counter0/Timer0
Index 5: Write/Read Counter1/Timer1
Index 6: Write/Read Counter2/Timer2
Index 7: Write Control word register of 8254

Base + 4: Status register , Read/Write , D7D6D5D4D3D2D1D0
Read operation:
D7: 1 -- EOC end of conversion
0 -- EOC not finished
D6: 0 -- bipolar mode.
1 -- Unipolar mode
D5: 1 -- Single-Ended AD
0 -- Differential AD
D4: 1 -- FIFO empty
0 -- FIFO not empty
D3: 1 -- FIFO half full
0 -- FIFO not half full
D2: 1 -- FIFO full
0 -- FIFO not full
D1: 1 -- BUSY . This bit is set to 1 when the scan sequence is not completed yet.
0 -- not busy
D0: 1 -- A/D enable
0 -- disable
Write: XD6D5XXXXD0
X--- don't care
D6: 1 -- Select unipolar mode
0 -- Select bipolar mode
D5: 1 -- Select single-ended analog input
0 -- Select differential analog input
D0: 1 -- arming the A/D conversion waiting for trigger signal to start operation.
0 -- disarm.

Base + 5: Interrupt status register. Read only D7D6D5D4D3D2D1D0

Read: D7 --- not used
D6 --- not used
D5 --- Terminal Count interrupt status
D4 --- Timer0/counter0 interrupt status
D3 --- External trigger interrupt status
D2 --- FIFO full interrupt status
D1 --- FIFO half full interrupt status
D0 --- End of scan interrupt status

Interrupt status bit : 1 for interrupt occurred, 0 not occurred.

Base + 6: 4-bit digital I/O Write/Read XXD5D4D3D2D1D0

D5: 1 ---select the external trigger from IP1/GS0/Trig
0 ---select the external trigger from IP0/Ext clock

D4: 1-- digital I/O on the main connector are used to select gain and channel of expansion board.
0-- disable expansion board

Write: D3D2D1D0 output 4-bit to output port located at main D37 pin 3, pin 22, pin 4, pin 23.

Read: D3D2D1D0 Read the input port located at main D37 pin 5, pin 24, pin 6, pin 25.

Base + 7: Reserved

Base + 8, 9 : DAC0 D/A channel 0 output port

Write only: D15D1 4 -------D4D3D2D1D0
16-bit

Base + A,B: DAC1 D/A channel 1 output port

Write only: D15D14 ---------D4D3D2D1D0
16-bit

Base + C..F: 82C55 Programmable Peripheral Interface chip

Base+ C: PIO Port A
Base +D: PIO Port B
Base +E: PIO Port C
Base +F: PIO Control word

Base + 8000 : Board enable /disable

Read: disable the DAQ-1101/1102

Any read to Base +8000 will cause DAQ board to be disable.

Write: enable the DAQ-1101/1102

Any write to Base +8000 will cause DAQ board to be enable.

* Example--analog trigger

If you prefer to write your own code for the data acquisition system in stead of using the DAQDRIVE software driver, the example below illustrates the procedure you have to follow to perform an analog trigger data acquisition:

a) Set the analog threshold voltage (or triggered voltage) by sending its value to DAC1 (analog output channel 1 located at Base+A)

b) Program the index 0 register :

D3: 0 analog trigger
D2: single/continuous
D1: 0 external trigger
D0: rising/trailing edge trigger

c) Flush the data and scan FIFO ---Index 2 register.

d) Program the scan sequence of each channel and gain ---writing the words to Base+0,1.

e) Program the 82C54 for the sampling rate at Index register 4..7

f) Arm the circuit by writing D0=1 to Base +4.

After the above procedures are executed, the board will be waiting for triggering by comparing the threshold voltage with the analog input voltage at the start channel.